

REMARKS

The Examiner's Action mailed on February 27, 2006, has been received and its contents carefully considered.

In this Amendment, Applicants have editorially amended claims 1, 3, 5 and 6, and cancelled claim 2 without prejudice. Claim 1 is the only independent claim, and claims 1 and 3-10 are pending in the application. For at least the following reasons, it is submitted that this application is in condition for allowance.

The drawings were objected to for failing to show reference element 28. Replacement and annotated drawing sheets are submitted herewith showing 'main logic circuit 28', and it is therefore respectfully submitted that the objection to the drawings be withdrawn.

Claims 2 and 3 were rejected under 35 USC §112, ¶2 for failing to particularly point out and distinctly claim the subject matter that Applicants regard as their invention. These rejections are respectfully traversed.

The features of claim 2 have now been incorporated into claim 1, but "the different digital level" has been amended to "different digital levels" in claim 1. Similarly, "the required clock type" in claim 3 has been changed to "a required clock type".

As regards the meaning of claim 3, this claim has been amended to recite "said identification signals identify a required clock type to said clock

generator module". It is believed that this clarifies the original wording without changing the meaning, and that this is consistent with the specification.

Claims 1 and 7-10 were rejected under 35 USC §103(a) as obvious over *Chang et al.* (US 6,006,327) in view of *Speiser et al.* (US 5,454,725). This rejection is moot in light of the incorporation of the features of claim 2 into claim 1.

Claims 2-6 were rejected under 35 USC §103(a) as obvious over *Chang et al.* in view of *Speiser et al.* and further in view of *Huang et al.* (US 2003/0126483). This rejection is respectfully traversed.

Independent claim 1 as amended has essentially the same scope as cancelled claim 2, reciting essentially the same features.

Chang et al. teaches an option setting device and method where "the CPU **210** issues a user-selected clock rate setting via the chip set **220** to the clock generator **250**" as shown in FIG. 2. The Office Action admits in ¶9 that "Chang et al fail to detail the method used to identify the different types of modules".

Speiser et al., on the other hand, teaches a method of identifying Network Interface Cards (NICs), as quite distinct from clock generator modules.

¶[0002] of *Huang et al.* in fact states:

[0002] Please refer to FIG. 1. FIG. 1 shows the block diagram for the computer starter of the ATX computer system in the prior art. It was also taught by the U.S. Pat. No. 6,128,744. A computer starter and starting method for the ATX computer system provided in U.S. Pat. No. 6,128,744 includes a power supply 10, a smart

card interface 12, a clock generator 14, a micro-controller 16, a non-volatile memory 18, and a power control circuit 20. In this model, the computer starter utilizes the 5V standby voltage when the AXT computer system is turned off as a voltage source of the computer starter. In this embodiment, the smart card interface 12 can be a card reader. When the smart card is inserted into a smart card interface 12, a PRESENT signal is activated to generate an enable signal En to inform the computer and other peripherals. The clock generator 14 is driven by the enable signal En to generate a reference clock CLKS, and the micro-controller 16 is driven by the reference clock CLKS to read out the user identification signal stored in the smart card. The user identification includes at least an identity and a corresponding password for a user. In the non-volatile memory 18 is stored a plural of computer identification signals. The non-volatile memory 18 can be memory or an electrically erasable programmable read-only memory. When micro-controller 16 is driven by the reference clock CLK.sub.S to output a reset signal (RST), a power voltage (V.sub.DDCARD), a clock signal (CLK.sub.CARD), and I/O signals through the smart card 12. These signals are used to reset the smart card, read the user identification signal stored in the smart card, and generate a verification signal (V.sub.ON) to the power control circuit 20 when the computer identification signal stored in the non-volatile memory matches the user identification signal stored in the smart card. The power control circuit 20 will output a start signal (PS_ON#) to the AXT power supply of the AXT computer system in response to the received verification signal (V.sub.ON) so as to turn on the AXT computer system.

This paragraph, which relates to prior art known to *Huang et al.*, essentially teaches, among other things, sensing the presence of a smart card, and turning

on a power supply if the smart card is present, but does not teach or suggest that “said mainboard provides power supply to said clock generator module” as actually claimed in the present invention.

In actual fact, the clock generator **14** of *Huang et al.*'s prior art FIG. 1 must already be running before the power control circuit **20** outputs the start signal, because the output of the clock generator **14** is used in reading the smart card. Quoting from the cited paragraph “the computer starter utilizes the 5V standby voltage”, but there is no indication where the standby voltage comes from.

Huang et al. also fails to teach or suggest other features imported into claim 1 from original claim 2, which are also taught by neither *Chang et al.* nor *Speiser et al.*

Neither *Chang et al.*, nor *Speiser et al.*; nor *Huang et al.* teach or suggest that “said reference clock input signal selectively receives a clock reference input from a selected reference clock source” as presently claimed in claim 1, not least because none of the references teaches a reference clock source external to a clock generator. See, in a non-limiting example, ¶[0021] of the specification, which reads in pertinent part “The reference clock input of the clock generator module **10** can be selected to be from the external clock input contact **22**, on-board reference clock source **27**, or the reference clock

generated by the clock generator module 10 itself". Hence, the reference clock input is not merely a control input, but an input to which an actual reference clock source is applied, and none of the applied references show this.

It is submitted that this application is in condition for allowance. Such action and the passing of this case to issue are requested.

Should the Examiner feel that a conference would help to expedite the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Should any fee be required, however, the Commissioner is hereby authorized to charge the fee to our Deposit Account No. 18-0002, and advise us accordingly.

Respectfully submitted,



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ALP

AMENDMENT

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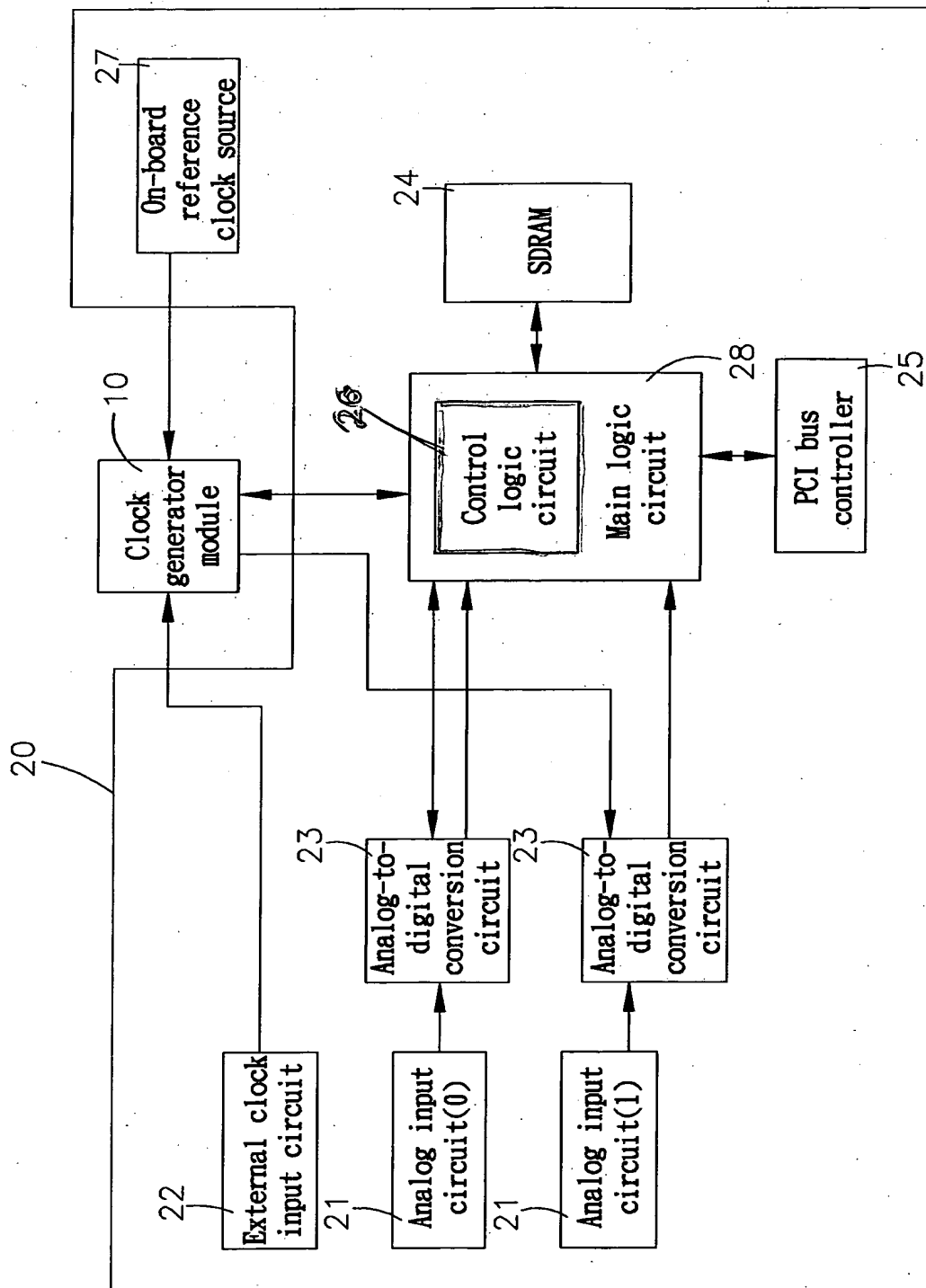


FIG. 3